

***"ALWAYS COMPLETE"***

**Cogent CSB337  
Atmel AT91RM9200  
OEM Single Board Computer**

**Hardware Reference Manual**

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**Cogent Computer Systems, Inc.**

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# 1 WARRANTY

The enclosed product ("the Product"), a part of the Cogent Modular Architecture or Cogent Single Board series, is warranted by Cogent Computer Systems, Inc. ("Cogent") for a period of six months for reasonable development testing and use, all as further described and defined below. This warranty runs solely to the individual or entity purchasing the Product and is not transferable or assignable in any respect. This warranty is valid only for so long as the product is used intact as shipped from Cogent. Any attempt or effort to alter the Product, including but not limited to any attempt to solder, desolder, unplug, replace, add or affix any part or component of or onto the Product, other than components specifically intended for the user to plug and unplug into appropriate sockets and/or connectors to facilitate user programming and development, all as specifically described and authorized in the Cogent Customer Product Users Manual, shall void this warranty in all respects. Coverage under this warranty requires that the Product be used and stored at all times in conditions with proper electrostatic protection necessary and appropriate for a complex electronic device. These conditions include proper temperature, humidity, radiation, atmosphere and voltage (standard commercial environment, 0C to +70C, <60%RH). Any Product that has been modified without the express, prior written consent of Cogent is not covered by this warranty. Cogent Single Board and Cogent Modular Architecture test and bus connectors are for use with Cogent adapters only. The use or connection of any test or bus connector, adapter or component with any device other than a Cogent connector or adapter shall void this warranty and the warranty of all other components, parts and modules connected to the rest of the system. Cogent shall not be responsible for any damage to the Product as a result of a customer's use or application of circuitry not developed or approved by Cogent for use on or in connection with the Product.

This warranty does not cover defects caused by electrical or temperature fluctuations or from stress resulting from or caused by abuse, misuse or misapplication of the Product. Any evidence of tampering with the serial number on the Product shall immediately void this warranty. This Product is not intended to be used on or embedded in or otherwise used in connection with any life sustaining or life saving product and this warranty is not applicable nor is Cogent liable in any respect if the Product is so used. Notwithstanding anything to the contrary herein, Cogent expressly disclaims any implied warranty of merchantability or implied warranty of fitness for a particular purpose in connection with the manufacture or use of the Product.

## 2 OVERVIEW

### 2.1 INTRODUCTION

The CSB337 was designed and developed by Cogent Computer Systems, Inc. as a highly integrated Atmel AT91RM9200 Single Board Computer. Based upon the ARM920T Core, the CSB337 provides a powerful, flexible platform for software design and development, microprocessor evaluation, embedded control systems, and much more. The major features of the CSB337 are as follows:

- 180Mhz Atmel AT91RM9200 ARM920T CPU with 16K I-Cache and 16K D-Cache
- 32Mbyte 32-Bit Wide SDRAM (Micron MT48LC8M16-7TG or equivalent)
- 8Mbyte 16-Bit Wide Intel 28F640J3A (or equivalent) StrataFLASH
- Epson S1D13706 320x240 LCD Controller with Internal 80K Frame Buffer
- Dual RS-232 Serial Ports, one with complete handshaking
- 3 Additional Serial Ports via GPIO Expansion Connector, TTL interface, no handshaking
- USB Device Interface (Dual USB Host Interface via GPIO Expansion Connector)
- 10/100 Ethernet Interface via Internal MAC with LXT971A PHY
- Dallas DS1307 (or 3.3V equivalent DS1338) Real Time Clock With 56Byte NVRAM
- Infineon SAK82C900 Dual CAN Controller via SPI
- Secure Digital (SD) Card Socket via Internal SDIO Controller (4-Bit)
- Compact Flash Interface (socket provided on User Board)
- I2S Codec Interface via GPIO Expansion Connector
- 16-Bit High Speed Embedded Trace Port via 38-Pin Mictor Connector
- 26-Pin JTAG Header
- User Readable 4 Position DIP Switch
- 40-Pin Press fit Header for CPU Data, Address, GPIO, I2S, USB, Compact Flash and SPI
- Dedicated 40-Pin Press fit Header for LCD Controller
- Dedicated 50-Pin Press fit Header for Front Panel I/O Connectors (RJ45, DB-9, etc.)
- 5V Only Power @ <1A
- Very Small 3.5" x 3.2" Board can be mounted directly onto User PCB

### 2.2 REFERENCE DOCUMENTS

Refer to the following documents for more detailed information regarding the major components of the CSB337. In all cases, you should contact the manufacturer for the latest documentation (including errata) regarding these components.

1. "ARM920T™- based Microcontroller AT91RM9200 User's Manual", DOC1768A
2. "3V Intel StrataFLASH Memory" Datasheet, Order # 290667-006
3. Epson S1D13706 "Embedded Memory LCD Controller" Technical Manual, Document number: X31B-Q-001-06

4. Intel LXT971A *“3.3V Dual-Speed Fast Ethernet Transceiver”* Datasheet, Order # 249414-001
5. Dallas DS1307 *“2-Wire RTC with 56-Byte NVRAM”* Datasheet
6. Infineon *“SAK82C900 Stand Alone TwinCAN Controller”* Datasheet V1.0D3

## 3 ON-BOARD I/O DEVICES

### 3.1 CSB337 ADDRESS MAP

The following table describes the Address Map of the CSB337. Refer to the AT91RM9200 documentation for information regarding on-chip peripheral addressing.

CPU Chip Select	Chip Select Width	Wait States	Address Start	Address End	Description
See Notes	-	-	0x0000.0000	0x000F.FFFF	1 <sup>st</sup> 1Mbyte StrataFlash or 16Kbyte Internal SRAM
N/A	32	1	0x0200.0000	0x0200.3FFF	16Kbyte Internal SRAM
*CS0	16	10	0x1000.0000	0x10FF.FFFF	StrataFlash
*CS1	32	N/A	0x2000.0000	0x21FF.FFFF	32Mbyte SDRAM
*CS2	16	WAIT	0x3000.0000	0x300F.FFFF	Epson S1D13706
*CS3	N/A	N/A	0x4000.0000	0x4FFF.FFFF	Expansion Chip Select 0
*CS4	8/16	N/A	0x5000.0000	0x5FFF.FFFF	Compact Flash Chip Enable 1
*CS5	N/A	N/A	0x6000.0000	0x6FFF.FFFF	Compact Flash Chip Enable 1
*CS6	N/A	N/A	0x7000.0000	0x7FFF.FFFF	Compact Flash Chip Enable 2
*CS7	N/A	N/A	0x8000.0000	0x8FFF.FFFF	Expansion Chip Select 1

Table 1 – CSB337 Address Map

#### Address Map Notes:

1. The AT91RM9200 also maps the first 1Mbyte of \*CS0 to address 0x0000.0000. This allows the CPU to boot from Flash after reset. The user may write one to the re-map bit (RCB, Bit 0) in the Remap Control Register (0xFFFF.FF00) to map the Internal SRAM to 0x0000.0000.
2. The Micromonitor Ethernet code uses most of the internal SRAM (0x0020.0000) for it's buffers starting at offset 0x100 (256 bytes). If you re-map the SRAM to address 0 in order to allow for ram based exception vectoring, care must be taken that the vectors and any exception handling code occupy only the first 256 bytes of the SRAM.
3. WAIT in the "Wait States" column indicates the device uses the \*WAIT input to control the access. All other values are those programmed by the Boot Monitor. The Compact Flash and Expansion Chip Selects are not enabled by default.

4. All addresses not listed here are reserved.
5. Many devices do not fully map their entire allotted address space. However, for future compatibility, do not access the devices outside of their address ranges listed here.
6. Compact Flash Chip Select (\*CS4) is not actually used in hardware. It is provided by the AT91RM9200 as a convenience for controlling the external Address and Data Buffers required to interface to a Compact Flash Socket. Cogent recommends using the CF Card Detect Signals to control the CF Address buffers and the Card Detect Signals plus the Read Strokes (\*CF\_IOR and \*CF\_OE) to control the data buffers. This is the method used on the CSB301 Development Platform. Software must still assign \*CS4 to the Compact Flash function even though the signal is not used. This is done by setting the CS4A bit in the EBI Chip Select Assignment Register.
7. After reset, a 1Mbyte alias of the Flash is located at address 0. The reset code should jump from there to the proper Flash address of 0x1000.0000 as soon as possible.

### **3.2 8MBYTE STRATAFLASH**

The CSB337 uses an Intel StrataFlash 28F128-J3A device (or equivalent) for boot memory. CS0 must be set to 16-bits width (this is the default on reset using hardware strapping) and 10 wait states (the default is 64 wait states after reset).

### **3.3 32MBYTE SDRAM**

The CSB337 uses two Micron MT48LC8M16 devices (or equivalent) for system memory. The specifications of these devices provides for 100Mhz operation. The AT91RM9200 operates them at a maximum of 61Mhz allowing CAS Latency 2 and RAS to CAS 2 modes to be set.

### **3.4 EPSON S1D13706 LCD/CRT CONTROLLER**

The CSB337 uses the S1D13706 to provide video output to LCD or CRT displays. The following table describes the address map of the S1D13706 resources.

Address Start	Address End	Description
0x3000.0000	0x3000.01FF	S1D13706 Control Registers
0x3004.0000	0x3006.FFFF	80Kbyte Video Buffer

Table 2 – S1D13706 Address Map

S1D13706 Interface Notes:

1. The S1D13706 is connected to \*CS2 as a 16-bit wide device with 4 wait states

minimum and external Wait enabled.

2. The S1D13706 interface is set for Generic, Little Endian Mode using Hardware Strapping.
3. Software must clear the Host Access Disable bit in the S1D13706 Miscellaneous Register prior to accessing any other S1D13706 locations.

### **3.5 INTEL LXT971 PHY**

An LXT971A PHY is used to interface the AT91RM9200 10/100 Ethernet controller to a 10/100 network via standard twisted pair wire. The LXT971A controls two LED indicators via programmable LED drivers. The default setting of these drivers is to display Speed on E\_LED1 and Link Status on E\_LED2. Software needs to change the setting for LED2 to display combined Link Status and RX/TX Activity. Writing a value of 0x0BFA into the LXT971A LED Control Register (0x14) will accomplish this. Refer to the AT91RM9200 User Manual for more information on reading/writing to the LXT971A PHY via the MII Bus. The interrupt signal from the LXT971 is connected to GPIO PC2.

### **3.6 SPI BUS**

The AT91RM9200 provides a sophisticated, multi-slave SPI Bus implementation. On the CSB337, one of the SPI chip selects is used, while the others are made available on the GPIO Expansion Connector. SPI\_CS0 selects the SAK82C900 TwinCAN Controller and SPI\_CS1 is for User Expansion. SPI\_CS2 and SPI\_CS3 are also available on the GPIO Expansion Connector. They are shared with UART3 TXD and RXD.

### **3.7 INFINEON SAK82C900 DUAL CAN CONTROLLER**

The Infineon SAK82C900 TwinCAN Controller allows the CSB337 to act as a CAN Hub or Master controller. Each channel operates independently and software may choose to use one or both as the application determines. The device is located on the SPI bus and is selected using SPI Chip Select 0. Channel 0's interrupt is routed to GPIO PC4 while Channel 1's interrupt is routed to GPIO PC5. The connections between the CAN transceivers and the Front Panel Connector as shown in the following table.

CAN Signal	Description	P6 Pin
CAN_A+	CAN Channel A, Positive Data Line	45
CAN_A-	CAN Channel A, Negative Data Line	46
CAN_B+	CAN Channel B, Positive Data Line	49
CAN_B-	CAN Channel B, Negative Data Line	50

Table 3 – Dual CAN to Front Panel Connector Assignments

SAK82C900 Interface Notes:

1. The maximum clock rate for the SAK82C900 is 6Mhz.
2. There is an errata for the SAK82C900 that require the user to enable “Baud-Rate-Error Enable” detection when there are multiple SPI slaves on the bus with the SAK82C900.
3. Each channel has a jumper that allows the user to determine the termination method. If the jumper is in, then a 120 ohm resistor is placed across the two bus differential signals. Removing the jumper removes the termination. Typically the two devices at the ends of the bus are terminated, while the rest are not.

### ***3.8 SD/MMC CARD***

A single “Secure Digital/Multi-Media Card”, socket is located on the CSB337. Using it’s high speed 4-Bit SDIO controller, the AT91RM9200 can interface to a wide variety of memory and I/O cards including Bluetooth and 802.11 I/O. The socket is connected to AT91RM9200 SD Card Controller A and may be interfaced at speeds up to 25Mbits per second. Actual speed depends upon the card and system loading, with practical rates limited to 4-8Mbits per second (x4 for 4-bit I/O). AT91RM9200 GPIO’s PD5 and PD6 provide SD card detection (0 = card inserted) and write protect detection (0 = card is write protected) respectively.

### ***3.9 2-WIRE INTERFACE***

The AT91RM9200 contains a high-speed DMA capable Two-Wire Interface. The signals are shared with GPIO PA26 (SCL) and GPIO PA25 (SDA). This allows for a simpler “bit-bang” interface to be implemented as an option. This is the method used in Micromonitor. Refer to the Micromonitor source code for examples of using this method. Both signals are made available on the GPIO Expansion Connectors (P4) and the LCD Interface Connector (P5) for maximum flexibility.

### ***3.10 DALLAS DS1307 REAL-TIME CLOCK***

The DS1307 is connected to the 2-wire bus at address 0x68. This device provides clock/calendar functions as well as 56 bytes of RAM. A 3.6V lithium cell provides power to the DS1307 when board power is off. Life expectancy of the cell is 10 years at 25°C.

# 4 AT91RM9200 ON-CHIP I/O DEVICES

## 4.1 OVERVIEW

The AT91RM9200 has a number of on-chip peripheral devices as well as a number of user defined control lines. While it is beyond the scope of this document to provide detailed programming and interfacing information for the AT91RM9200 on-chip peripherals, the following section describes the assignments for these devices and control lines as implemented on the CSB337.

## 4.2 AT91RM9200 CHIP SELECTS

As described in Section 3.1, the AT91RM9200 Chip Selects are used to enable the various peripheral devices on the CSB337. As a cross-reference they are described again in the following table.

Chip Select	Attached Device(s)	Notes
CS0	StrataFLASH	Boot Device
CS1/SDCS	SDRAM	
CS2	S1D13706 LCD Controller	
CS3	Expansion Connector	*XCS0
CS4	Compact Flash Chip Select	Not used in hardware
CS5	Compact Flash Chip Enable 1	*CE1 to C/F Socket
CS6	Compact Flash Chip Enable 2	*CE2 to C/F Socket
CS7	Expansion Connector	*XCS1

Table 4 – AT91RM9200 Chip Select Assignments

## 4.3 AT91RM9200 GENERAL PURPOSE I/O PORT PIN ASSIGNMENTS

The AT91RM9200 has four 32-Bit General Purpose I/O Registers, Port A, B, C and D. The usage is described in the following table. Note that it is the responsibility of software to setup these bits for the correct direction and default state as well as the assignment of alternate functions.

Port A GPIO Assignments				
Bit	DIR	Signal	Connection	Notes

Port A GPIO Assignments				
Bit	DIR	Signal	Connection	Notes
PA0	In	SPI_DIN	SAK82C900 & P4, Pin 7	On Rev. P4 and lower, there is a conflict that prevents the use of SPI DIN for external devices. DO NOT CONNECT.
PA1	Out	SPI_DOUT	SAK82C900 & P4, Pin 8	
PA2	Out	SPI_CLK	SAK82C900 & P4, Pin 6	
PA3	Out	SPI_CS0	SAK82C900	
PA4	Out	SPI_CS1	P4, Pin 5	
PA5	Out	TXD3	P4, Pin 17	UART3 Transmit or SPI Chip Select 2
PA6	In	RXD3	P4, Pin 18	UART3 Receive or SPI Chip Select 3
PA7	In	E_TXCLK	LXT971A	Ethernet Transmit Clock
PA8	Out	E_TXEN	LXT971A	Ethernet Transmit Enable
PA9	Out	E_TXDO	LXT971A	Ethernet Transmit Data 0
PA10	Out	E_TXD1	LXT971A	Ethernet Transmit Data 1
PA11	In	E_CRS	LXT971A	Ethernet Carrier Sense
PA12	In	E_RXD0	LXT971A	Ethernet Receive Data Bit 0
PA13	In	E_RXD1	LXT971A	Ethernet Receive Data Bit 1
PA14	In	E_RXER	LXT971A	Ethernet Receive Error
PA15	Out	E_MDC	LXT971A	Ethernet MII Clock
PA16	I/O	E_MDIO	LXT971A	Ethernet MII Data
PA17	I/O	PA17	P4, Pin 12	GPIO or UART 0 Transmit
PA18	I/O	PA18	P4, Pin 11	GPIO or UART 0 Receive
PA19	I/O	PA19	P4, Pin 10	GPIO or UART 0 CTS
PA20	I/O	PA20	P4, Pin 9	GPIO or UART 0 RTS
PA21	In	USR_SW2	P6, Pin 24	User Pushbutton Switch 2
PA22	In	RXD2	P4, Pin 19	UART 2 Transmit or Direct IRQ3
PA23	Out	TXD2	P4, Pin 20	UART 2 Receive or Timer 2, I/O B

Port A GPIO Assignments				
Bit	DIR	Signal	Connection	Notes
PA24	Out	USB_SCON	USB DDP	1 = USB 12Mbit connect condition on the USB device port
PA25	I/O	SDA	P4, Pin 4 & P5, Pin 38	Two-Wire Data – Routed to LCD Expansion Connector as well as GPIO Expansion Connector
PA26	I/O	SCL	P4, Pin 3 & P5, Pin 37	Two-Wire Clock – Routed to LCD Expansion Connector as well as GPIO Expansion Connector
PA27	Out	SD_CK	SD Socket	SD/MMC Card Controller A Clock
PA28	Out	SD_CMD	SD Socket	SD/MMC Card Controller A Command
PA29	I/O	SD_D0	SD Socket	SD/MMC Card Controller A Data Bit 0
PA30	In	DBG_RXD	P6, Pin 7	Debug UART Receive (via RS-232 Transceiver)
PA31	Out	DBG_TXD	P6, Pin 9	Debug UART Transmit (via RS-232 Transceiver)

**Table 5 – AT91RM9200 GPIO Port A Pin Assignments**

Port B GPIO Assignments				
Bit	DIR	Signal	Connection	Notes
PB0	Out	*LED2	P6, Pin 29	Low True LED Enable
PB1	Out	*LED1	P6, Pin 28	Low True LED Enable
PB2	Out	*LED0	P6, Pin 27	Low True LED Enable
PB3	I/O	SD_D1	SD Socket	SD/MMC Card Controller A Data Bit 1
PB4	I/O	SD_D2	SD Socket	SD/MMC Card Controller A Data Bit 2
PB5	I/O	SD_D3	SD Socket	SD/MMC Card Controller A Data Bit 3
PB6	-	N/C		Unavailable for use
PB7	I/O	TK1	P4, Pin 37	I2S Transmit Clock
PB8	Out	TD1	P4, Pin 34	I2S Transmit Out (To Codec)
PB9	In	RD1	P4, Pin 35	I2S Receive Data (From Codec)
PB10	I/O	RK1	P4, Pin 38	I2S Receive Clock

Port B GPIO Assignments				
Bit	DIR	Signal	Connection	Notes
PB11	Out	RF1	P4, Pin 36	I2S Receive Frame Sync (To Codec)
PB12	Out	E_TXD2	LXT971A	Ethernet Transmit Data 2
PB13	Out	E_TXD3	LXT971A	Ethernet Transmit Data 3
PB14	In	E_TXER	LXT971A	Ethernet Transmit Error
PB15	In	E_RXD2	LXT971A	Ethernet Receive Data 2
PB16	In	E_RXD3	LXT971A	Ethernet Receive Data 3
PB17	In	E_RXDV	LXT971A	Ethernet Receive Data Valid
PB18	In	E_COL	LXT971A	Ethernet Collision
PB19	In	E_RXCK	LXT971A	Ethernet Receive Clock
PB20	Out	TXD1	P6, Pin 17	Via RS-232 Transceiver
PB21	In	RXD1	P6, Pin 15	Via RS-232 Transceiver
PB22	I/O	PB22	P4, Pin 33	PB22 or *CF_IOIS16
PB23	In	DCD1	P6, Pin 13	Via RS-232 Transceiver
PB24	In	CTS1	P6, Pin 18	Via RS-232 Transceiver
PB25	In	DSR1	P6, Pin 14	Via RS-232 Transceiver
PB26	Out	RTS1	P6, Pin 16	Via RS-232 Transceiver
PB27	Out	PCK0	P2, Pin 38	Bus Clock or GPIO
PB28	In	*USR_SW1	P6, Pin 23	User Pushbutton Switch 1
PB29	In	*USR_SW0	P6, Pin 22	User Pushbutton Switch 0

**Table 6 – AT91RM9200 GPIO Port B Pin Assignments**

Port C GPIO Assignments				
Bit	DIR	Signal	Connection	Notes
PC0	In	*XINT0	P2, Pin 32	External Interrupt 0 or GPIO
PC1	In	*XINT1	P2, Pin 33	External Interrupt 1 or GPIO
PC2	In	*PHY_INT	LXT971A	Ethernet PHY Interrupt
PC3	In	*CF_CD	P4, Pin 16	Compact Flash Card Detect or GPIO
PC4	In	*CAN_INT0	SAK82C900	Can Controller Channel 0 interrupt

Port C GPIO Assignments				
Bit	DIR	Signal	Connection	Notes
PC5	In	*CAN_INT1	SAK82C900	Can Controller Channel 1 interrupt
PC6	In	*WAIT	P2, Pin 34	External Wait (Low True) or GPIO
PC7	I/O	A23	P2, Pin 26 & FLASH	CPU Address Bus 23
PC8	I/O	A24	FLASH	CPU Address Bus 24
PC9	-	-	-	Unavailable for Use
PC10	-	-	-	Unavailable for Use
PC11	Out	*CF_CE1	P4, Pin 26	Compact Flash Chip Enable 2 or GPIO
PC12	Out	*CF_CE2	P4, Pin 27	Compact Flash Chip Enable 2 or GPIO
PC13	Out	*CS7	P2, Pin 28	Expansion Chip Select 1 or GPIO
PC14	In	RI1	P6, Pin 20	Via RS-232 Transceiver
PC15	In	DTR1	P6, Pin 19	Via RS-232 Transceiver
PC16	I/O	D16	P1, Pin 19	CPU Data Bus Bit 16
PC17	I/O	D17	P1, Pin 20	CPU Data Bus Bit 17
PC18	I/O	D18	P1, Pin 21	CPU Data Bus Bit 18
PC19	I/O	D19	P1, Pin 22	CPU Data Bus Bit 19
PC20	I/O	D20	P1, Pin 23	CPU Data Bus Bit 20
PC21	I/O	D21	P1, Pin 24	CPU Data Bus Bit 21
PC22	I/O	D22	P1, Pin 25	CPU Data Bus Bit 22
PC23	I/O	D23	P1, Pin 26	CPU Data Bus Bit 23
PC24	I/O	D24	P1, Pin 27	CPU Data Bus Bit 24
PC25	I/O	D25	P1, Pin 28	CPU Data Bus Bit 25
PC26	I/O	D26	P1, Pin 29	CPU Data Bus Bit 26
PC27	I/O	D27	P1, Pin 30	CPU Data Bus Bit 27
PC28	I/O	D28	P1, Pin 31	CPU Data Bus Bit 28
PC29	I/O	D29	P1, Pin 32	CPU Data Bus Bit 29
PC30	I/O	D30	P1, Pin 33	CPU Data Bus Bit 30
PC31	I/O	D31	P1, Pin 34	CPU Data Bus Bit 31

Table 7 – AT91RM9200 GPIO Port C Pin Assignments

Port D GPIO Assignments				
Bit	DIR	Signal	Connection	Notes
PD0	I/O	PD0	P4, Pin	GPIO
PD1	I/O	PD0	P4, Pin	GPIO
PD2	I/O	PD0	P4, Pin	GPIO
PD3	-	-	-	Unavailable for Use
PD4	-	-	-	Unavailable for Use
PD5	In	*SD_CD	SD Socket	SD Card Detect
PD6	In	*SD_WP	SD Socket	SD Write Protect
PD7	Out	ETM_SYNC	P3, Pin 32	Embedded Trace Module Sync
PD8	Out	ETM_CLK	P3, Pin 6	Embedded Trace Module Clock
PD9	Out	ETM_PS0	P3, Pin 38	Embedded Trace Module CPU Status 0
PD10	Out	ETM_PS1	P3, Pin 36	Embedded Trace Module CPU Status 1
PD11	Out	ETM_PS2	P3, Pin 34	Embedded Trace Module CPU Status 2
PD12	Out	ETM_PK0	P3, Pin 30	Embedded Trace Module Data Bit 0
PD13	Out	ETM_PK1	P3, Pin 28	Embedded Trace Module Data Bit 1
PD14	Out	ETM_PK2	P3, Pin 26	Embedded Trace Module Data Bit 2
PD15	Out	ETM_PK3	P3, Pin 24	Embedded Trace Module Data Bit 3
PD16	Out	ETM_PK4	P3, Pin 22	Embedded Trace Module Data Bit 4
PD17	Out	ETM_PK5	P3, Pin 20	Embedded Trace Module Data Bit 5
PD18	Out	ETM_PK6	P3, Pin 18	Embedded Trace Module Data Bit 6
PD19	Out	ETM_PK7	P3, Pin 16	Embedded Trace Module Data Bit 7
PD20	Out	ETM_PK8	P3, Pin 37	Embedded Trace Module Data Bit 8
PD21	Out	ETM_PK9	P3, Pin 35	Embedded Trace Module Data Bit 9
PD22	Out	ETM_PK10	P3, Pin 33	Embedded Trace Module Data Bit 10
PD23	Out	ETM_PK11	P3, Pin 31	Embedded Trace Module Data Bit 11
PD24	Out	ETM_PK12	P3, Pin 29	Embedded Trace Module Data Bit 12
PD25	Out	ETM_PK13	P3, Pin 27	Embedded Trace Module Data Bit 13

Port D GPIO Assignments				
Bit	DIR	Signal	Connection	Notes
PD26	Out	ETM_PK14	P3, Pin 25	Embedded Trace Module Data Bit 14
PD27	Out	ETM_PK15	P3, Pin 23	Embedded Trace Module Data Bit 15

Table 8 – AT91RM9200 GPIO Port D Pin Assignments

**4.4 AT91RM9200 INTERRUPT PIN ASSIGNMENTS**

The AT91RM9200 has a number of direct interrupt inputs to the Advanced Interrupt Controller. The AT91RM9200 also allows any GPIO to be assigned as an interrupt. The following table describes the direct interrupt inputs as well as any GPIO that are being used as interrupts on the CSB337. Note that all of the interrupts are shared with GPIO and are assigned as GPIO inputs by Micromonitor. User software is required to enable the interrupt function for any signal.

GPIO	Source	Notes
PB29	User Switch 0	Low True (Can be assigned as Direct Interrupt IRQ0)
PB28	User Switch 1	Low True (Can be assigned as Direct Interrupt FIQ)
PA21	User Switch 2	Low True
PC0	Expansion Interrupt 0	Application Specific
PC1	Expansion Interrupt 1	Application Specific
PC2	LXT971A 10/100 PHY	Low True
PC4	SAK82C900 CAN Channel 0	Low True
PC5	SAK82C900 CAN Channel 1	Low True

Table 9 – AT91RM9200 Interrupt Pin Assignments

**4.5 AT91RM9200 UARTS**

The AT91RM9200 has 5 UARTS for up to 1 Mbps asynchronous serial communications. Two of these, Debug UART (no handshaking) and UART 1 (full handshaking) are routed to the Front Panel Connector (via RS-232 Transceivers) as Serial 0 and Serial 1, respectively. UART 0 (CTS/RTS handshaking) and UART's 2 & 3 (no handshaking) are available on the GPIO Expansion Connector (TTL signals only). The serial clock for all UARTS is sourced from the internal CPU Master Clock (MCK). Refer to the AT91RM9200 Users Manual for more information. The following table describes the usage of the Debug UART and UART 1 signals.

Signal	Description	Connection	Notes
DBG_TXD	Debug UART TXD	P6, Pin 9	Latches BMS Input at boot time
DBG_RXD	Debug UART RXD	P6, Pin 7	
TXD1	UART 1 TXD	P6, Pin 17	
RXD1	UART 1 RXD	P6, Pin 15	
DCD1	UART 1 DCD	P6, Pin 13	
CTS1	UART 1 CTS	P6, Pin 18	
DSR1	UART 1 DSR	P6, Pin 14	
RTS1	UART 1 RTS	P6, Pin 16	
DTR1	UART 1 DTR	P6, Pin 19	GPIO PC15
RI1	UART 1 RI	P6, Pin 20	GPIO PC14

Table 10 – AT91RM9200 UART Signal Assignments

#### 4.6 AT91RM9200 10/100 ETHERNET MAC

The AT91RM9200 supports a 10/100MBit Ethernet interface via an internal Media Access Controller (MAC). This MAC is interfaced via external pins to an LXT971A 10/100 PHY. Refer to the AT91RM9200 Users Manual for detailed programming information. Micromonitor uses the internal SRAM as the location of the Transmit and Receive buffers for the Ethernet MAC. This is required for proper operation of the MAC when running from Flash with the caches off. The following table describes the usage of the Ethernet MAC signals.

Signal	Description	Notes
E_TXD0-3	Ethernet Transmit Bus	To LXT971A PHY
E_TXCK	Ethernet Transmit Clock	From LXT971A PHY
E_TXEN	Ethernet Transmit Enable	To LXT971A PHY
E_TXER	Ethernet Transmit Error	To LXT971A PHY
E_RXD0-3	Ethernet Receive Bus	From LXT971A PHY
E_RXCK	Ethernet Receive Clock	From LXT971A PHY
E_RXER	Ethernet Receive Error	From LXT971A PHY

Signal	Description	Notes
E_RXDV	Ethernet Receive Data Valid	From LXT971A PHY
E_COL	Ethernet Collision	From LXT971A PHY
E_CRS	Ethernet Carrier Sense	From LXT971A PHY
E_MDC	Ethernet MII Clock	To LXT971A PHY
E_MDIO	Ethernet MII Data	Bi-directional

**Table 11 – AT91RM9200 Ethernet MAC Signal Assignments**

**4.7 AT91RM9200 SPI CONTROLLER**

The AT91RM9200 provides a high speed, multi-slave Serial Peripheral Interface (QSPI) controller. This controller can interface with multiple slaves with minimal host intervention. The internal AT91RM9200 DMA controller can be used to transfer data between the SPI controller and system memory for very high data rates. The SPI clock can be programmed up to MCK/2. The following table describes the usage of the SPI signals.

Signal	Description	Notes
SPI_CLK	SPI Clock	Maximum Clock Determined by Slowest Slave on the Shared bus
SPI_DOUT	SPI Data Out to Slave	
SPI_DIN	SPI Data In from Slave	
SPI_CS0	SPI Chip Select 0	Routed to SAK82C900 CAN
SPI_CS1	SPI Chip Select 1	Routed to GPIO Expansion Connector
SPI_CS2	SPI Chip Select 2	Routed to GPIO Expansion Connector as TXD3
SPI_CS3	SPI Chip Select 3	Routed to GPIO Expansion Connector as RXD3

**Table 12 – AT91RM9200 SPI Signal Assignments**

**4.8 AT91RM9200 SD/MMC CONTROLLER**

The AT91RM9200 provides a high speed Secure Digital (SD/MMC) controller. This controller can interface with MMC, SD and SDIO Cards with minimal host intervention. The internal AT91RM9200 DMA controller can be used to transfer data between the SD/MMC Socket on the CSB337 and system memory for very high data rates. The SD/MMC clock can be programmed up to MCK/2. The following table describes the

usage of the SD/MMC signals.

Signal	Description	Notes
SD_CK	SD Clock	
SD_CMD	SD Command	
SD_D0-3	SD Data Bus	1–Bit for MMC, 1 or 4-Bit for SD and SDIO
SD_CD	SD Card Detect	Connected to GPIO PD4 0 = Card Inserted)
SD_WP	SD Write Protect	Connected to GPIO PD4 0 = Write Protected)

Table 13 – AT91RM9200 SD/MMC Signal Assignments

**4.9 AT91RM9200 COMPACT FLASH INTERFACE**

The AT91RM9200 supports the Compact Flash Interface using the internal Static Memory Controller. This requires certain GPIO and Chip Select signals to be assigned to the CF function. The following table describes the usage of the CF signals.

CF Socket Signal	Description	AT91RM9200 Signal	Connector #, Pin #
CF_D0-15	16-Bit Data Bus	D0-15	P1, Pins 3-18
CF_A0-10	11 Bit Address Bus	A0-10	P2, Pins 4-13
*CF_REG	CF Register enable	A22	P4, Pin 25
*CF_CE1	CF Chip Enable 1	*CS5	P4, Pin 26
*CF_CE2	CF Chip Enable 2	*CS6	P4, Pin 27
*CF_IOR	CF I/O Read Strobe	*BE1	P4, Pin 28
*CF_IOW	CF I/O Write Strobe	*BE2	P4, Pin 29
*CF_OE	CF Memory Read Strobe	*OE	P4, Pin 30
*CF_WE	CF Memory Write Strobe	*WE	P4, Pin 31
*CF_WAIT	CF Wait Request	*WAIT	P4, Pin 32
*CF_CD	CF Card Detect	GPIO PC3	P4, Pin16
*CF_IN	CF Interrupt ( or RDY)	Users choice	P2, Pin 32 or Pin 34

Table 14 – AT91RM9200 Compact Flash Signal Assignments

AT91RM9200 Compact Flash Interface Notes:

1. The Data, Address and Control signals must be buffered on the users board.

The \*CF\_CD signal can be used as an output enable for all buffers. An “OR” of the \*CF\_OE and \*CF\_IOR signals can be used to enable the direction of the data buffer to read (direction is out to CF when both are high). Refer to the CSB301 schematics for an example of how this is done.

2. The AT91RM9200 provides a \*CF\_CS signal (shared with \*CS4). While this signal is not physically used, software must still assign \*CS4 to the Compact Flash function. This is done by setting the CS4A bit in the EBI Chip Select Assignment Register.
3. It is possible to route the Compact Flash Interrupt (also known as CF\_RDY) to any one of the unused GPIO signals (as the AT91RM9200 allows any GPIO to generate an interrupt). However, for compatibility with other CSB3xx boards, it is advised to use one of the four interrupt enabled GPIO's on P4 (GPIO\_0 to GPIO\_3) or one of the two external interrupts on P2.

#### ***4.10 AT91RM9200 USB DEVICE PORT***

The AT91RM9200 has a single, USB 1.1 compliant Device Port. The two data signals are routed to the Front Panel Connector (P6) via a pair of 33 ohm resistors. Additionally, a 1.5K ohm resistor is connected from the USB Positive Data signal to GPIO PA24 (USB\_SCON). When the USB device port is connected to a USB host, software can indicate to the host that a device is present by driving PA24 to a 1. This indicates both the presence of USB device and that the device is 12Mbit capable. This also allows the AT91RM9200 USB Device software to delay recognition by the Host until it is ready.

#### ***4.11 AT91RM9200 DUAL USB HOST PORTS***

The AT91RM9200 has two, USB1.1 compliant, Host Ports. The data signals for these ports are routed to the GPIO Expansion Connector (P4) via 33 ohm series resistors and each data signal also has a 15K pull down resistor. The proper connection to the USB Type A connector, including port power management, must be done on the user's board. The data bits are connected to the GPIO Expansion Connector as follows:

Signal	Description	P4 Pin
HDP A	USB Host Port A, Positive Data Line	21
HDMA	USB Host Port A, Negative Data Line	22
HDP B	USB Host Port B, Positive Data Line	23
HDMB	USB Host Port B, Negative Data Line	24

Table 15 – AT91RM9200 USB Host Signal Assignments

## 5 CSB337 SOFTWARE

### *5.1 OVERVIEW*

Due to the various resources contained on the CSB337, both on and off the AT91RM9200, it is necessary to initialize a large number of AT91RM9200 registers and external devices before correct operation can begin. These values and their proper sequencing is beyond the scope of this document. The Micromonitor source code should be referred to as the best guide.

# 6 CONNECTORS AND PINOUTS

## 6.1 OVERVIEW

This section provides the locations, descriptions and pinouts of the various connectors on the CSB337.

## 6.2 CONNECTOR LOCATIONS

The following diagram shows the location of the Connectors, Switches and Option Jumpers on the CSB337.

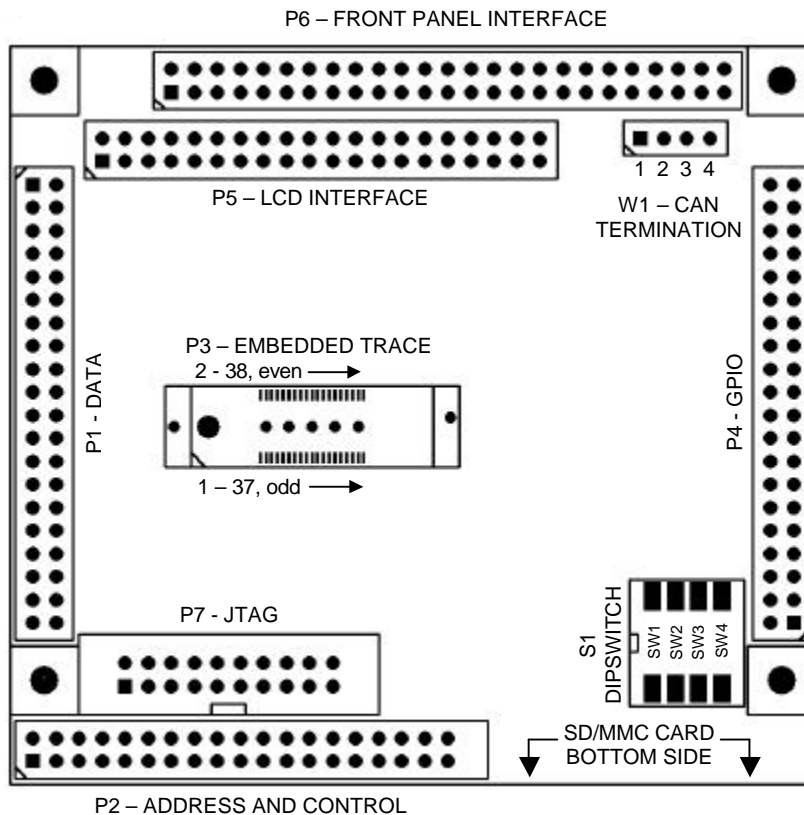
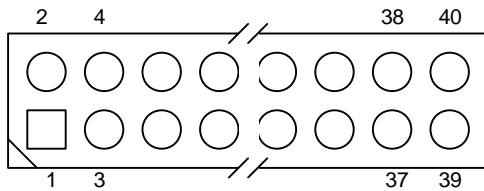


Figure 1 - CSB337 Connector Locations

## 6.3 PRESSFIT CONNECTORS

P1 through P5 are 40-Pin pressfit connectors, while P6 is a 50-Pin pressfit connector. They all have a female socket on the bottom of the board and a male header on the top. They are all pinned out as follows (note that P6 has 50 pins):



The slash in the silkscreen and the square pad indicate Pin 1.

#### 6.4 P1, DATA CONNECTOR

P1 is a 40-Pin Pressfit connector that carries the AT91RM9200 Data Bus. The following table describes the pinout of P1. The Signal indicates the usage as defined by Cogent for the CSB337.

Pin	Signal	Pin	Signal
1	+5V	2	+5V
3	D0	4	D1
5	D2	6	D3
7	D4	8	D5
9	D6	10	D7
11	D8	12	D9
13	D10	14	D11
15	D12	16	D13
17	D14	18	D15
19	D16	20	D17
21	D18	22	D19
23	D20	24	D21
25	D22	26	D23
27	D24	28	D25
29	D26	30	D27
31	D28	32	D29
33	D30	34	D31
35	*BE0/A0	36	*BE1
37	*BE2/A1	38	*BE3

Pin	Signal	Pin	Signal
39	GND	40	GND

Table 16 – P1, Data Connector Pinout

**6.5 P2, ADDRESS/CONTROL CONNECTOR**

P2 is a 40-Pin Pressfit connector that carries the AT91RM9200 Address Bus and Control signals. The following table describes the pinout of P2. The Signal indicates the usage as defined by Cogent for the CSB337. Where these signals are also available as GPIO, the GPIO port and bit are shown in parenthesis.

Pin	Signal	Pin	Signal
1	+5V	2	+5V
3	A0	4	A1
5	A2	6	A3
7	A4	8	A5
9	A6	10	A7
11	A8	12	A9
13	A10	14	A11
15	A12	16	A13
17	A14	18	A15
19	A16	20	A17
21	A18	22	A19
23	A20	24	A21
25	A22	26	A23
27	*CS3	28	*CS7 (PC13)
29	*WE	30	*OE
31	*WE	32	GPIO PC0
33	GPIO PC1	34	*WAIT (PC6)
35	N.C.	36	*RST
37	GND	38	PCK0 (PB27)

Pin	Signal	Pin	Signal
39	GND	40	GND

Table 17 – P2, Address/Control Connector Pinout

### 6.6 P4, GPIO CONNECTOR

P4 is a 40-Pin Pressfit connector that carries the AT91RM9200 GPIO as well as the 2-Wire and SPI interface signals. The following table describes the pinout of P4. The Signal name indicates the primary usage as defined by Cogent for the CSB337. Alternate functions (if available) are shown in parenthesis.

Pin	Signal	Pin	Signal
1	+5V	2	+5V
3	SCL (GPIO PA26)	4	SDA (PA25)
5	SPI_CS1 (PA4)	6	SPI_CLK (PA2)
7	SPI_DIN (PA0)	8	SPI_DOUT (PA1)
9	PA20	10	PA19
11	PA18 (RXD0)	12	PA17 (TXD0)
13	PD0	14	PD1
15	PD2	16	PC3
17	TXD3 (PA5)	18	RXD3 (PA6)
19	TXD2 (PA23)	20	RXD2 (PA22)
21	HDP A (USB Host A D+)	22	HDMA (USB Host A D-)
23	HDP B (USB Host B D+)	24	HDMB (USB Host B D-)
25	A22 (used as *CF_REG)	26	CS5 (*CF_CE1)
27	CS6 (*CF_CE2)	28	*BE1 (*CF_IOR)
29	*BE3 (*CF_IOW)	30	*OE (*CF_OE)
31	*WE (*CF_WE)	32	*WAIT (*CF_WAIT)
33	PB22 (*CF_IOIS16)	34	I2S TD (PB8)
35	I2S RD (PB9)	36	I2S RF (PB11)
37	I2S TK (PB7)	38	I2S RK (PB10)
39	GND	40	GND

Table 18 – P4, GPIO Connector Pinout

**6.7 P5, LCD INTERFACE CONNECTOR**

P5 is a 40-Pin Pressfit connector that carries the S1D13706 LCD Controller signals. The following table describes the pinout of P5.

Pin	Signal	Pin	Signal
1	GND	2	GND
3	+5V	4	+5V
5	FD17	6	FD16
7	FD15	8	FD14
9	FD13	10	FD12
11	FD11	12	FD10
13	FD9	14	FD8
15	FD7	16	FD6
17	FD5	18	FD4
19	FD3	20	FD2
21	FD1	22	FD0
23	FPSHIFT	24	FPLINE
25	FPFRAME	26	DRDY
27	GPIO4	28	CVOUT
29	PWMOUT	30	GPIO0
31	GPIO1	32	GPIO2
33	GPIO3	34	MOD
35	N.C.	36	TOUCH *IRQ (Routed to AT91RM9200 GPIO PD4)
37	SCL	38	SDA
39	GND	40	GND

Table 19 – P5, LCD Interface Connector Pinout

**6.8 P6, FRONT PANEL INTERFACE CONNECTOR**

P6 is a 50-Pin Pressfit connector that carries the CSB337 I/O signals for the various

interfaces such as Ethernet, RS-232, CAN, etc. It is expected that these signals will go directly to the designated connector (DB9, RJ45, etc.), Switch or LED. However, the user is free to implement these connections in whatever manner is appropriate for their application. The following table describes the pinout of P6. Refer to the CSB300 Breakout board manual an example of how to use this connector. Note that DTR\_B and RI\_B are derived from GPIO PC15 and PC14 respectively.

P6 Pin	CSB337 Signal	Front Panel Connector & Pin	P6 Pin	CSB337 Signal	Front Panel Connector & Pin
1	+5V	Power In	2	+5V	Power In
3	GND	GND	4	GND	GND
5	-	DB9_A-1	6	-	DB9_A-6
7	RXD_A	DB9_A-2	8		DB9_A-7
9	TXD_A	DB9_A-3	10		DB9_A-8
11	-	DB9_A-4	12	-	DB9_A-9
13	DCD_B	DB9_B-1	14	DSR_B	DB9_B-6
15	RXD_B	DB9_B-2	16	RTS_B	DB9_B-7
17	TXD_B	DB9_B-3	18	CTS_B	DB9_B-8
19	DTR_B	DB9_B-4	20	RI_B	DB9_B-9
21	*RST_IN	RESET SW.	22	*IRQ (PB29)	USER SW0
23	*FIQ (PB28)	USER SW1	24	PA21	USER SW2
25	GND	SW COMM.	26	+3V	PWR_ON LED
27	PB2	USER LED0	28	PB1	USER LED1
29	PB0	USER LED2	30	+3V	LED COMM.
31	USB_D-	USB-2	32	USB_D+	USB-3
33	E_LINK/ACT	E_LED2	34	E_SPEED	E_LED1
35	E_GND	E_GND	36	E_TX+	RJ45-1
37	E_GND	E_GND	38	E_TX-	RJ45-2
39	E_GND	E_GND	40	E_RX+	RJ45-3
41	E_GND	E_GND	42	E_RX-	RJ45-6
43	E_GND	E_GND	44	GND	GND

P6 Pin	CSB337 Signal	Front Panel Connector & Pin	P6 Pin	CSB337 Signal	Front Panel Connector & Pin
45	CAN_A+	DB9_C-7	46	CAN_A-	DB9_C-2
47	GND	GND	48	GND	GND
49	CAN_B+	DB9_D-7	50	CAN_B-	DB9_D-2

Table 20 – P6, Front Panel Interface Connector Pinout

**6.9 P3, EMBEDDED TRACE MODULE CONNECTOR**

P3 is a 38-Pin (with integral ground plane) Mictor connector, AMP Part #767054-1. Mating part number is AMP Part #767003-9. The following table details the pin assignments of this connector.

P3 Pin	CSB337 Signal	P3 Pin	CSB337 Signal
1	N.C.	2	N.C.
3	N.C.	4	N.C.
5	Ground	6	ETM_CLK
7	Pull down via 10	8	N.C.
9	*RESET (to CPU)	10	Pull Up via 10K
11	TDO	12	+3V
13	TCK	14	+3V
15	TCK	16	ETM_PK7
17	TMS	18	ETM_PK6
19	TDI	20	ETM_PK5
21	*TRST (to CPU)	22	ETM_PK4
23	ETM_PK15	24	ETM_PK3
25	ETM_PK14	26	ETM_PK2
27	ETM_PK13	28	ETM_PK1
29	ETM_PK12	30	ETM_PK0
31	ETM_PK11	32	ETM_SYNC
33	ETM_PK10	34	ETM_PS2

P3 Pin	CSB337 Signal	P3 Pin	CSB337 Signal
35	ETM_PK9	36	ETM_PS1
37	ETM_PK8	38	ETM_PS0

**6.10 P7, JTAG CONNECTOR**

P7 is a 20-Pin Shrouded Male Dual Row .1” Header. The following table details the pin assignments of this connector.

P7 Pin	CSB337 Signal	P7 Pin	CSB337 Signal
1	+3V	2	+3V
3	*TRST (to CPU)	4	Ground
5	TDI	6	Ground
7	TMS	8	Ground
9	TCK	10	Ground
11	N.C.	12	Ground
13	TDO	14	Ground
15	*RESET (to CPU)	16	Ground
17	N.C.	18	Ground
19	N.C.	20	Ground

Table 21 – P7, JTAG Connector Pinout

**6.11 W1, CAN TERMINATION SELECT**

W1 is a 4-Pin single row header that allows the user to enable/disable the 120 ohm termination for each CAN port. Pins 1-2 control CAN0, while 3-4 Control CAN1. A jumper installed places a 120 ohm resistor across the CAN\_H and CAN\_L lines for that port. This is usually done on the two end ports on the entire bus.

**6.12 S1, 4 POSITION DIP SWITCH**

S1 is a 4-Position DIP switch. Each switch is connected between two SAK82C900 PIO signals as shown in the table below. P4-P7 are pulled high via resistors. To read a switch, software should drive P0-P4 low, then read the state of P4-P7. This was done as a way to test the SPI interface as well as providing the ability to read the switch.

Switch Position	SAK82C900 PIO Signals
1	P0 - P4
2	P1 - P5
3	P2 - P6
4	P3 - P7

Table 22 – S1, DIP Switch Connections



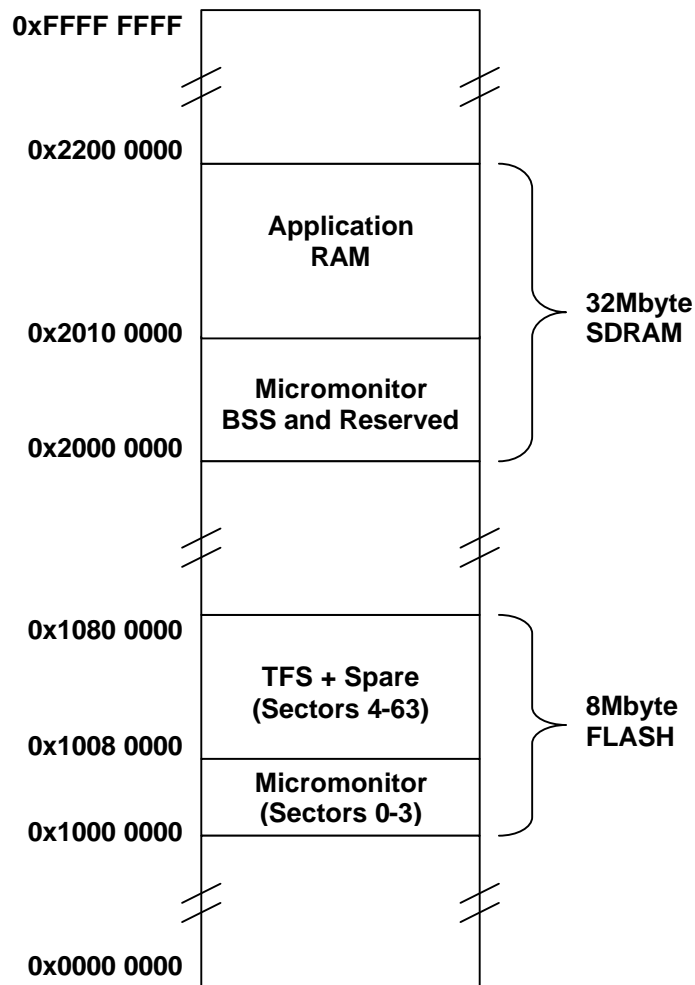
# 8 MICROMONITOR

## 8.1 INTRODUCTION TO MICROMONITOR

The CSB337 is delivered standard with the Micromonitor boot monitor in FLASH. Micromonitor was developed and is maintained by Ed Sutter of Lucent Technologies. Micromonitor is an open source product and may be copied, modified and re-used without restriction. However, neither Cogent nor Lucent is liable for any problems that may arise during the use of Micromonitor including its use with this board.

## 8.2 MICROMONITOR SOFTWARE MEMORY MAP

The memory usage by Micromonitor is shown in the following block diagram:



Note: All addresses shown are physical addresses.

### ***8.3 CONNECTING TO MICROMONITOR***

As delivered from Cogent, Micromonitor is configured to use UART 0 (DB9\_A on the Front Panel Interface connector). The default connection is 38,400 baud, 8-N-1, no handshaking. A null modem cable is provided with the CSB337 that will connect the CSB337 to another DTE port such as found on a PC.

Micromonitor also uses the Ethernet port to listen for connections via UDP.

### ***8.4 MICROMONITOR COMMANDS***

Micromonitor supports a wide variety of commands that allow the user to modify and/or read memory, download programs from Ethernet, Serial or on-board Flash File System (TFS) and many others. Refer to the Micromonitor Users Manual for a complete listing. Note that not all commands are available on all targets. Type the following command (assuming you are connected using a standard terminal program) at the Micromonitor command prompt to get a list of the commands currently enabled on your target:

```
umon> help
```

The terminal window will then display the commands installed on your target. Additional help for each command can be displayed by typing “help xxx” where “xxx” is the specific command you are seeking help on.

You can also type the following to get information regarding the build date, memory usage, default application load address (APPRAMBASE) and other useful information regarding Micromonitor as installed on your CSB337:

```
uMon> mstat
```

### ***8.5 GETTING MORE INFORMATION ABOUT MICROMONITOR***

Micromonitor reference information and a more advanced Micromonitor training guide are available from Microcross, Inc. ([www.microcross.com](http://www.microcross.com)).